Compact Model for Double-Gate Tunnel FETs With Gate–Drain Underlap

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***Abstract*— A compact model for double-gate tunnel FETs (TFETs) with gate–drain underlap (DG u-TFET) is proposed which accounts for the alleviation of ambipolar current and Miller capacitance (C_{dg}) compared with double-gate tunnel FETs (DG TFET). The ON-state current degradation caused by the underlap is reproduced by extending the ideal DG TFET model with an effective resistance between the channel and the drain. Based on the device surface potential, the terminal charge model is developed which enables the possibility of circuit simulation and the terminal capacitance is further derived from the definition. This model captures the electrical characteristics of DG u-TFET explicitly and good agreement is achieved compared with TCAD simulation. After the model is implemented into HSPICE, an inverter is established and successfully simulated without convergence problem.**

***Index Terms*— Ambipolar current, compact model, gate–drain underlap, tunneling field-effect transistor (TFET).**

I. Introduction

CONTINUOUS downscaling of the conventional MOSFETs has brought the issue of device power dissipation more considerable. Recently, the tunneling field-effect transistor (TFET) has attracted much attention as efficient energy saving device due to its superior subthreshold performance [1]–[5]. Nevertheless, to realize the application of TFET into circuit level, the ambipolar behavior should be well controlled [6]–[9]. Nowadays, the gate–drain underlap structure [10] has been effectively utilized in TFET (represented as u-TFET) to suppress the ambipolar current. Through simulation study, the feasibility of Miller capacitance (C_{dg}) reduction compared with conventional TFET has been demonstrated by Zhuge *et al.* [11] and the range of underlap ratio ($L_{underlap}/L_{channel}$) for device performance optimization has also been discussed in [12].

Some works on u-TFET continue in terms of performance estimation at circuit level by table look-up method. Vijayvargiya *et al.* [13] explored the analog/RF performance attributes of u-TFET for low-power applications. Avci *et al.* [14] compared the performance, switching energy, and process variations for u-TFET and MOSFET in logic. Biswas *et al.* [15] investigated the u-TFET as a capacitorless memory cell. In order to extend the huge potential of u-TFET in practical circuit implementation, a compact model available for SPICE is necessary. Recently, several TFET SPICE models have published [16]–[20]. Simultaneously, the impact of the gate–drain underlap has been found and studied by simulation, while not involved in model yet. Considering the accuracy requirement for circuit simulation, an SPICE compatible model for TFET with gate–drain underlap is urgently needed.

In this paper, a compact model for silicon-based double-gate TFETs with gate–drain underlap (DG u-TFET) that can be applied to all operation regions (positive/negative gate bias) is proposed for the first time. The description of ambipolar current is necessary due to the negative input from output voltage undershot (<0 V) [18] in multistage circuit. It is a complete model with both drain current and terminal charge/capacitance which is ready for circuit simulation. The model shows good accuracy compared with TCAD simulation and works properly in circuit simulator (HSPICE).

II. DG u-TFET Modeling Under Positive Gate Bias

Similar to double-gate DG TFET, the DG u-TFET is equivalent to a gated tunnel diode in series with a gate–drain underlapped DG MOSFET. To comprehensively model the surface potential for DG u-TFET, one extra Poisson's equation (PE) should be solved for the underlap. Although subthreshold analysis for gate–drain underlapped MOSFET has

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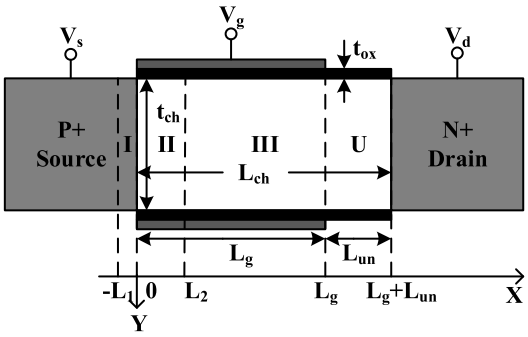

Fig. 1. Cross-sectional view of an n-type DG u-TFET. The gate dielectric is S_iO_2. The source and drain are heavily doped, while the channel is intrinsic.

been demonstrated [21]–[24], in the strong inversion condition, the PE in the underlap becomes unsolvable due to the nonuniform charge density. On the other hand, it has been reported that the underlap structure will increase the channel resistance and induce ON-state current degradation [10], [11]. Thus, a quantitative evaluation on the current degradation is needed for device performance optimization.

Instead of solving the PE, one possible way to consider the effect of the underlap is to model it as a series resistor, which is also applied in MOSFET modeling when the gate–source/drain underlap is introduced [25]–[27]. One main advantage of the resistor method is that it brings less extra computing burden than the coupling of DG TFET and DG underlapped MOSFET which is benefit for SPICE simulation. In the following work, it will be shown that by introducing a first-order resistor model, the ideal DG TFET model is extended for DG u-TFET, which reproduces the ON-state current degradation. Before this, a brief review on the surface potential model for DG TFET [17] is given below.

Fig. 1 shows the cross-sectional view of an n-type DG u-TFET. It is divided into four regions: source depleted region I, channel depleted region II, drift-diffusion region III, and underlap region U. Supposing that $L_{\rm un} = 0$, the device is reduced to a DG TFET. After solving the PEs, the surface potential in region I and region II can be, respectively, expressed as

$$\varphi_{s1}(x) = \frac{qN_{\rm seff}}{2\varepsilon_{\rm si}}(x + L_1)^2 \tag{1}$$

$$\varphi_{s2}(x) = (V_{\rm gs} - V_{\rm fbs}) - [V_{\rm gs} - V_{\rm fbs} - V_{\rm bi} - \varphi_{\rm dg}] \times \cosh\left(\frac{x - L_2}{\lambda}\right) \tag{2}$$

where $\varepsilon_{\rm si}$ is the relative permittivity of silicon, $N_{\rm seff} = N_s - 2\varepsilon_{\rm ox}(V_{\rm gs} - V_{\rm fbs})/(qt_{\rm ox}t_{\rm ch}\pi/2)$ is the effective source doping concentration, $V_{\rm fbs} = W_{\rm fgate} - W_{\rm fsource}$ is the flat band voltage, $\lambda = (\varepsilon_{\rm si}t_{\rm ch}t_{\rm ox}/(2\varepsilon_{\rm ox}))^{1/2}$ is the natural length of double-gate MOSFET [28], $V_{\rm bi}$ is the built-in potential of the source/channel junction, and $\varphi_{\rm dg}$ is the surface potential in region III that calculated by the method in [29]. Detailed steps to come to the solution of the PE in each region and their corresponding boundary conditions can be found in [17]. By matching the boundary conditions, the lengths of region I and II are further solved

$$L_1 = \sqrt{2\varepsilon_{\rm si}\varphi_s(0)/qN_{\rm seff}} \tag{3}$$

$$L_2 = \lambda \cosh^{-1}\left[-\frac{\varphi_s(0) - (V_{\rm gs} - V_{\rm fbs})}{(V_{\rm gs} - V_{\rm fbs}) - (V_{\rm bi} + \varphi_{\rm dg})}\right] \tag{4}$$

where $\varphi_s(0) =$

$$-\sqrt{[V_{\rm gs} - V_{\rm fbs} - (V_{\rm bi} + \varphi_{\rm dg})]^2 + 2(V_{\rm gs} - V_{\rm fbs})\Phi + \Phi^2} + (V_{\rm gs} - V_{\rm fbs} + \Phi), \quad \Phi = \frac{qN_{\rm seff}\lambda^2}{\varepsilon_{\rm si}}. \tag{5}$$

By finding the minimum tunneling distance in the light of the presented potential profile, the tunneling current can be further calculated using Kane's model [30]. Detailed procedures are also available in [17] and will not be further illustrated. Here, the ideal current for DG TFET is defined as $I_{\rm ds0}$.

Now, supposing that $L_{\rm un} \neq 0$, the underlap region behaves as a resistor. The effective resistance is given by a first-order model [31]

$$R_{\rm un} = \frac{L_{\rm un}}{q \cdot \mu_e \cdot n_{\rm un} \cdot W_g \cdot t_{\rm ch}} \tag{6}$$

where μ_e is the electron mobility, $n_{\rm un}$ is the average electron concentration in the underlap region, and W_g is the width of the gate. For a given $V_{\rm gs0}$ and $V_{\rm ds0}$, using ideal current $I_{\rm ds0}$ as initial solution, the voltage drop on the resistor is $I_{\rm ds0} \cdot R_{\rm un}$, which leads to the effective drain voltage for DG TFET: $V_{\rm ds,eff} = V_{\rm ds0} - I_{\rm ds0} \cdot R_{\rm un}$. Then, use $I_{\rm ds}(V_{\rm gs0}, V_{\rm ds,eff})$ to replace $I_{\rm ds0}$ and repeat the above process. Usually after two–three iterations, the drain current and the effective drain voltage will meet a convergence criterion for the final solution. As the effective drain voltage is obtained, surface potential for region I, II, and III (the DG TFET part) of DG u-TFET is also determined, which can be further used to calculate the terminal charge.

In device SPICE model, the terminal charge is needed for ac/transient simulation due to the charging and discharging process. Therefore, a terminal charge model for DG u-TFET is developed based on the aforementioned surface potential and the feasibility of expressing terminal charge in terms of terminal voltage has been verified [32]. Besides, the terminal capacitance is calculated by differentiating the terminal charge with respect to the terminal voltage, which reflects the impact of gate–drain underlap on the Miller capacitance.

Charge component of DG u-TFET includes charge in the source depletion region and the channel. Assuming that dopants are fully ionized, the depletion charge in region I can be calculated with

$$Q_s = -qN_{\rm seff}W_gL_1. \tag{7}$$

The channel charge is divided into two parts: the inversion charge beneath the gate and the inner fringe charge [33]. Due to the poor coupling between the source and the gate, charge in the channel is entirely injected from the drain side [18]. Before the device is saturated, the inversion charge is dominant in the whole channel charge. The saturation here means drain current is saturated by increasing the drain voltage. Since the inversion charge in region II is ignored [17] and the inversion charge

profile is approximately uniform before saturation, the total inversion charge can be calculated with Gauss's law

$$Q_{\text{ch\_inv}} = -2W_g t_{\text{ch}}(L_g - L_2)C_{\text{ox}}(V_{\text{gs}} - V_{\text{fbs}} - \varphi_{\text{dg}} - V_{\text{bi}}). \quad (8)$$

After the device is saturated, the inner fringing charge replaces the dominant role of the inversion charge. When the drain voltage is much higher than the gate voltage, electrons in the underlap region are almost depleted. This is different from DG TFET that only a narrow depletion forms near the channel/drain interface. In consequence, the maximum lateral electric field at the end of the channel can be approximated by

$$E_m = \frac{V_{\text{ds}} + V_{\text{bi,d}} - \varphi_{\text{dg}}}{\lambda + L_{\text{un}}} \quad (9)$$

where $V_{\text{bi},d}$ is the built-in potential of the drain/channel junction. This expression guarantees the consistency between DG u-TFET and DG TFET when L_{un} equals to zero. With the zero-field assumption in region III [17], the inner fringe charge can be calculated with Gauss' law

$$Q_{\text{ch\_inf}} = W_g t_{\text{ch}} \varepsilon_{\text{si}} E_m. \quad (10)$$

Therefore, the total channel charge is the summation of the two components

$$Q_{\text{ch}} = Q_{\text{ch\_inv}} + Q_{\text{ch\_inf}}. \quad (11)$$

Due to the charge neutrality condition, charge in the gate terminal is

$$Q_g = -(Q_s + Q_{\text{ch}}). \quad (12)$$

From the definition of terminal capacitance

$$C_{ij} = \frac{dQ_i}{dV_j} \quad (13)$$

the terminal capacitance C_{sg} and C_{dg} are given by

$$C_{\text{sg}} = \frac{\partial Q_s}{\partial V_{\text{gs}}}, \quad C_{\text{dg}} = \frac{\partial Q_d}{\partial V_{\text{gs}}} = \frac{\partial Q_{\text{ch}}}{\partial V_{\text{gs}}}. \quad (14)$$

Direct modeling for C_{sg} and $C_{\text{dg\_inf}}$ is also available to qualitatively understand the capacitance component

$$C_{\text{sg}} = 2W_g \frac{\varphi_{\text{dg}}}{V_{\text{gs}} - V_{\text{fbs}} - V_{\text{bi}}} \frac{\varepsilon_{\text{si}} t_{\text{ch}}}{2\lambda} \exp\left(-\frac{N_{\text{seff}} L_1}{N_s \lambda}\right) \quad (15)$$

$$C_{\text{dg\_inf}} = 2W_g \exp\left[-\frac{q(V_{\text{gs}} - V_{\text{fbs}} - V_{\text{bi}} - \varphi_{\text{dg}})}{kT}\right] \times \frac{2\varepsilon_{\text{si}}}{\pi} \ln\left[1 + \frac{t_{\text{ch}}}{2(t_{\text{ox}} + L_{\text{un}})} \sin\left(\frac{\pi}{2}\frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{si}}}\right)\right]. \quad (16)$$

III. DG u-TFET Modeling Under Negative Gate Bias

It has been illustrated that with gate–drain underlap, carrier tunneling rate under negative gate bias through channel/drain barrier decreases due to larger tunnel distance and reduced inside electric field [9]. In this condition, similar to Section II, DG u-TFET is divided into four regions (see Fig. 2): drain depleted region I, underlap region U, channel depleted region II, and drift-diffusion region III. In the following

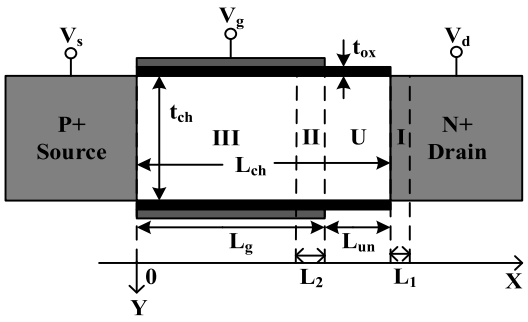

Fig. 2. Cross-sectional view of DG u-TFET under negative gate bias.

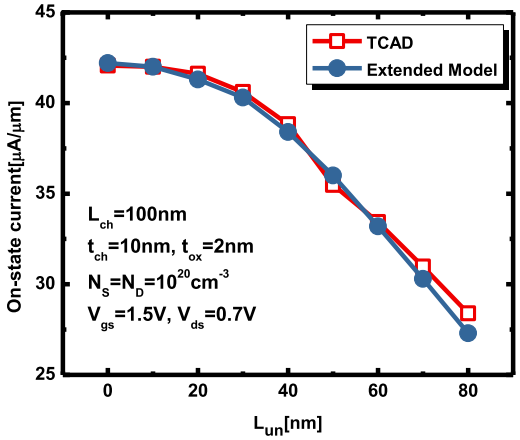

Fig. 3. Comparison between model-predicted on-state current and TCAD simulation by increasing L_{un} from 0 to 50 nm.

derivation, the surface potential is with reference to the channel Fermi level.

Due to the ultrathin body, potential along y-direction in region I and region U is assumed to be uniform. With the depletion approximation and neglecting the gate fringing field, surface potential in region I and region U can be calculated by solving the 1-D PE

$$\frac{d^2\varphi_{\text{sj}}(x)}{dx^2} = -\frac{qN_j}{\varepsilon_{\text{si}}} \quad (17)$$

where $j = 1, u$ which refers to region I and region U, respectively. The general form solution for (17) is easily obtained by integrating twice. Substituting the boundary conditions

$$\varphi_{s1}(L_{\text{ch}} + L_1) = V_D, \quad \frac{d\varphi_{s1}(x)}{dx}|_{x=L_{\text{ch}}+L_1} = 0 \quad (18)$$

where $V_D = V_{\text{bi},d} + V_{\text{ds}}$, the surface potential in region I is solved as

$$\varphi_{s1}(x) = \frac{-qN_D}{2\varepsilon_{\text{si}}}(x - L_{\text{ch}} - L_1)^2 + V_D. \quad (19)$$

Likewise, the surface potential in region U is obtained by matching the boundary conditions at $x = L_{\text{ch}}$

$$\varphi_{\text{su}}(L_{\text{ch}}) = \varphi_{s1}(L_{\text{ch}}), \quad \frac{d\varphi_{\text{su}}(x)}{dx}|_{x=L_{\text{ch}}} = \frac{d\varphi_{s1}(x)}{dx}|_{x=L_{\text{ch}}} \quad (20)$$

and its solution is

$$\varphi_{\text{su}}(x) = \frac{-qN_D}{2\varepsilon_{\text{si}}}L_1^2 + V_D - \frac{qN_D}{\varepsilon_{\text{si}}}L_1(L_{\text{ch}} - x). \quad (21)$$

Region II can be treated as a full-depletion region neglecting the inversion charge. Due to the double-gate structure, 2-D PE in region II is simplified with parabolic approximation [34] and transformed to the well-known form

$$\frac{d^2\varphi_{s2}(x)}{dx^2} - \frac{\varphi_{s2}(x) - (V_{\rm gs} - V_{\rm fbb})}{\lambda^2} = \frac{q \cdot N_{\rm ch}}{\varepsilon_{\rm si}} \tag{22}$$

where $V_{\rm fbb} = W_{\rm fgate} - W_{\rm fbody}$ is the flat band voltage, $N_{\rm ch}$ is the channel doping concentration, and $\lambda = (\varepsilon_{\rm si} t_{\rm ch} t_{\rm ox}/(2\varepsilon_{\rm ox}))^{1/2}$ is the natural length of double-gate MOSFET. The general form solution for (22) is given by

$$\varphi_{s2}(x) = A\exp\left(\frac{x-(L_g-L_2)}{\lambda}\right) + B\exp\left(-\frac{x-(L_g-L_2)}{\lambda}\right) + (V_{\rm gs} - V_{\rm fbb}). \tag{23}$$

By substituting the boundary conditions at $x = L_g - L_2$

$$\varphi_{s2}(L_g - L_2) = \varphi_s, \quad \frac{d\varphi_{s2}(x)}{dx}|_{x=L_g-L_2} = 0 \tag{24}$$

where φ_s is the surface potential in region III that calculated by the method in [22], (23) is transformed to

$$\varphi_{s2}(x) = [\varphi_s - (V_{\rm gs} - V_{\rm fbb})]\cosh\left(\frac{x-(L_g-L_2)}{\lambda}\right) + (V_{\rm gs} - V_{\rm fbb}). \tag{25}$$

The lengths of region I and region II can be derived using the continuity of surface potential at the boundaries. In this way, L_1 is calculated by solving the quartic equation as follows:

$$(V_D - V_{\rm gs} + V_{\rm fbb} - qN_DL_1L_u/\varepsilon_{\rm si} - qN_D/(2\varepsilon_{\rm si})L_1^2)^2 - (qN_D/\varepsilon_{\rm si}L_1\lambda)^2 = (\varphi_s - V_{\rm gs} + V_{\rm fbb})^2. \tag{26}$$

Because no analytical solution is available, L_1 is solved numerically, which can further lead to the length of region II

$$L_2 = \lambda\cosh^{-1}\left\{\frac{V_D - \frac{qN_D}{\varepsilon_{\rm si}}L_1L_u - (V_{\rm gs} - V_{\rm fbb})\frac{qN_D}{2\varepsilon_{\rm si}}L_1^2}{\varphi_s - V_{\rm gs} + V_{\rm fbb}}\right\}. \tag{27}$$

To obtain the minimum tunneling distance, it is vital to judge where the tunneling takes place. At low $|V_{\rm gs}|$, the tunneling distance is relatively large and the carriers may tunnel from region I to region II. In this condition, $W_{t,\min}$ is found to be

$$W_{t,\min} = X_1 - X_2 \tag{28}$$

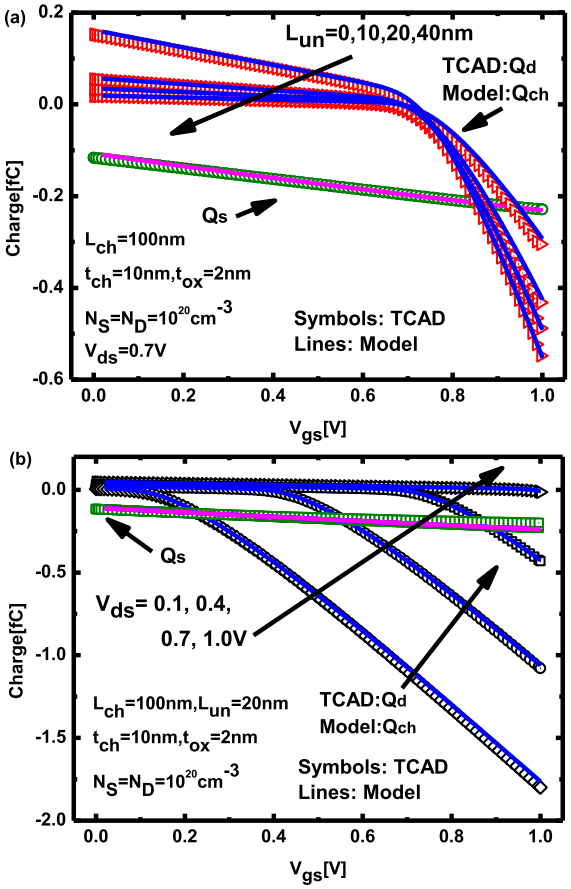

Fig. 4. Model-predicted charges versus TCAD simulation. (a) Predicted channel charge is identical with the simulated drain charge. (b) Charge components are compared from saturation to nonsaturation condition.

where (29)–(31), as shown at the bottom of the this page, X_1 and X_2 is the tunneling position in region I and region II, respectively, and $E_{gq} = E_g/q$. When X_2 is greater than L_g, tunneling occurs between region I and region U, and $W_{t,\min}$ is reduced to

$$W_{t,\min} = \frac{E_{gq}}{qN_DL_1}\varepsilon_{\rm si}. \tag{32}$$

According to Kane's model, the peak tunneling generation rate is written as

$$G_{\rm tun,max} = A \cdot \frac{E_g^{3/2}}{q^2} \cdot \frac{1}{W_{t,\min}^2}\exp\left(-\frac{W_{t,\min}}{\lambda_{\rm tun}}\right) \tag{33}$$

$$X_1 = L_{\rm ch} + L_1 - \sqrt{\frac{2\varepsilon_{\rm si}(V_D - \psi_I - E_{gq})}{qN_D}} \tag{29}$$

$$X_2 = \lambda\cosh^{-1}\left(\frac{\psi_I - V_{\rm gs} + V_{\rm fbb}}{\varphi_s - V_{\rm gs} + V_{\rm fbb}}\right) + L_g - L_2 \tag{30}$$

$$\psi_I = V_{\rm gs} - V_{\rm fbb} + \frac{q\lambda^2N_D}{\varepsilon_{\rm si}} + \sqrt{\left(\frac{q\lambda^2N_D}{\varepsilon_{\rm si}}\right)^2 + (V_{\rm gs} - V_{\rm fbb} - \varphi_s)^2 + \frac{2q\lambda^2N_D}{\varepsilon_{\rm si}}(V_D - V_{\rm gs} + V_{\rm fbb} - E_{gq})} \tag{31}$$

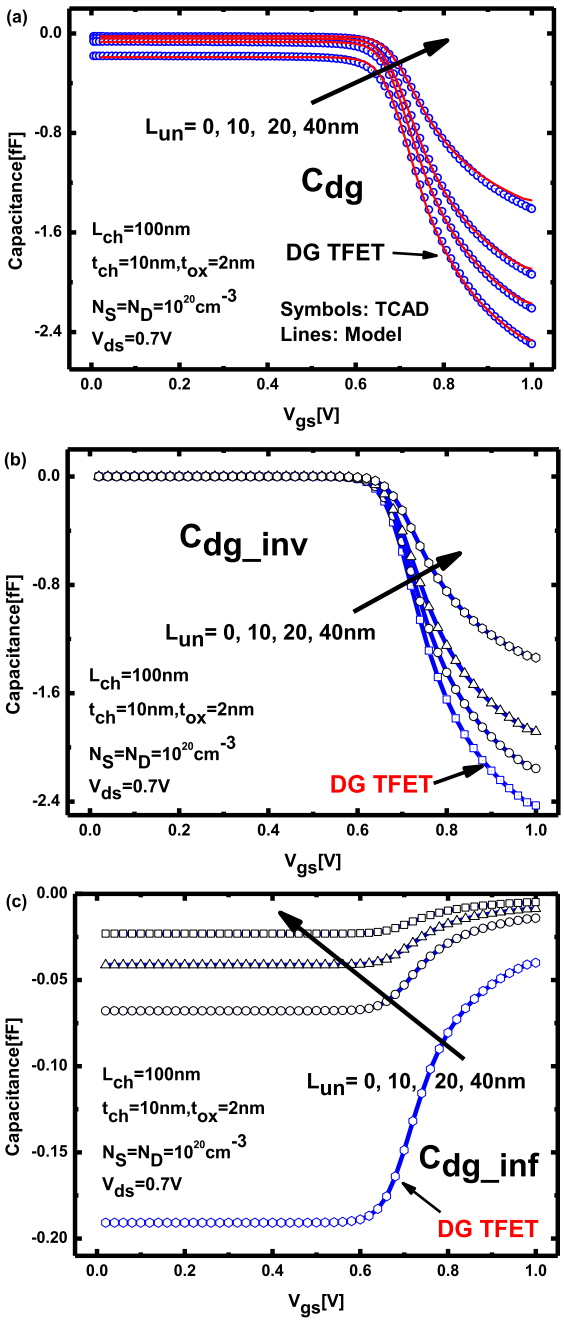

Fig. 5. (a) Model-predicted capacitance versus TCAD simulation with different L_{un}. (b) and (c) show the tendency that C_{dg_inv} and C_{dg_inf} change with increasing L_{un}.

where $\lambda_{tun} = 1/(q \cdot B \cdot E_g^{1/2})$, and drain current is then calculated by integrating the electron tunneling generation rate from $X = -\infty$ to $X = +\infty$

$$I_{ds,amb} = \frac{2W_g t_{ch} G_{tun,max}}{B\sqrt{E_{gq}}}. \tag{34}$$

A correction factor (35) of Fermi level is multiplied to (34) to avoid the nonzero current at $V_{ds} = 0$ and guarantee the current continuity

$$f_{fermi} = 2\left\{\frac{1}{2} - 1/\left[1 + \exp\left(\frac{qV_{ds}}{f_n \cdot kT}\right)\right]\right\}. \tag{35}$$

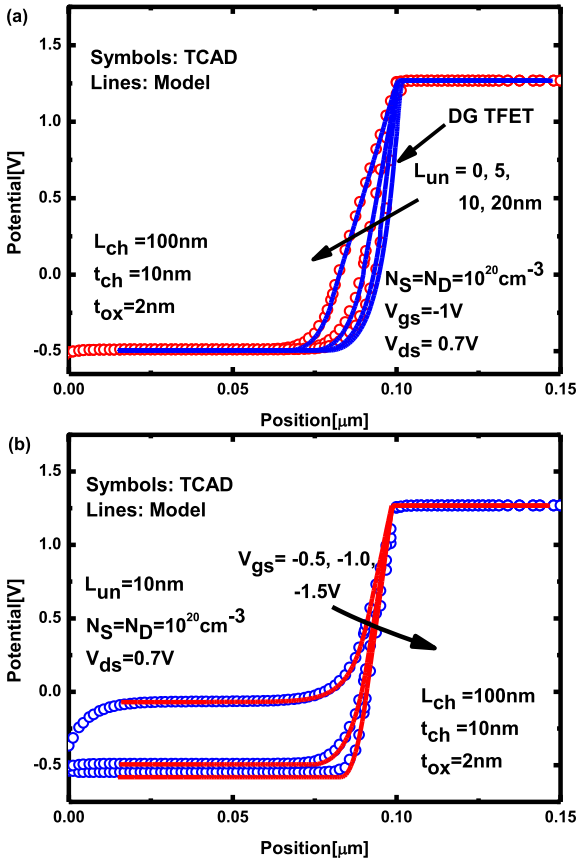

Fig. 6. Model-predicted surface potential versus TCAD simulation in negative gate bias condition. (a) Different L_{un}. (b) Different V_{gs} at L_{un}=10nm.

IV. Results and Discussion

The model-predicted values are compared with TCAD simulation for validation. The device simulation setup includes dynamic nonlocal path band to band tunneling model, Shockley–Read–Hall recombination model, and Fermi statistics. Device parameters are consistent for all groups of simulation except L_{un}.

The ON-state current degradation of DG u-TFET varying the underlap distance is shown in Fig. 3 and it is seen to reproduce the current degradation with an acceptable accuracy. This extended model indicates that the current degradation is related to both the ideal current I_{ds0} and the underlap distance L_{un}. On the one hand, larger L_{un} brings bigger series resistance so that drain voltage drops more on the underlap; on the other hand, if I_{ds0} is originally very large, like in heterojunction TFETs (H-TFET) or the applied gate voltage is very high, higher voltage drop is also expected on the underlap. For H-TFETs, this degradation can be evident even at a small gate voltage.

The terminal charge of DG u-TFET is plotted in Fig. 4. Fig. 4(a) shows that, compared with DG TFET, when increasing the underlap distance, the gate length is diminished thus reducing the effective area for inversion charge. The maximum electric field near the drain side becomes smaller that the inner fringe charge is also reduced. However, the source charge is barely affected by the gate–drain underlap, as the source depletion width mainly depends on the doping profile.

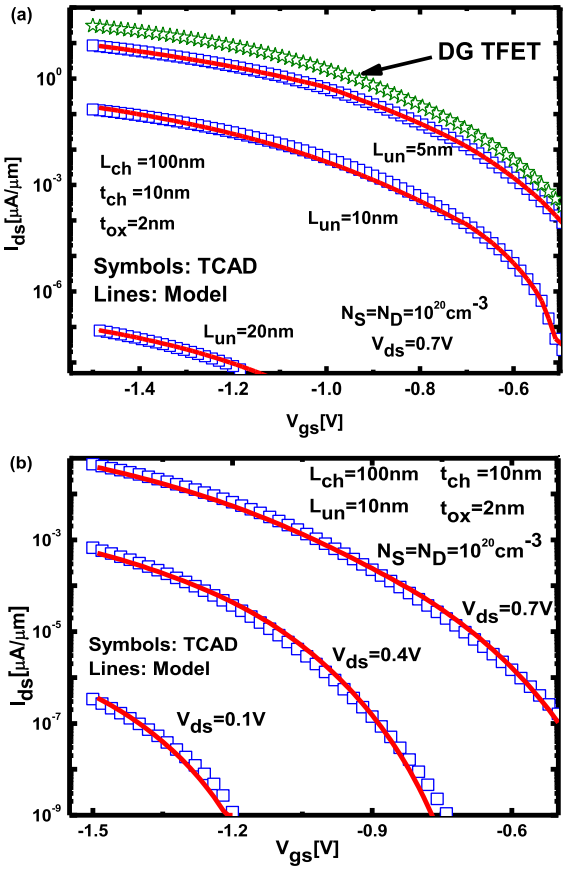

Fig. 7. Model-predicted ambipolar current versus TCAD simulation. (a) Different L_{un}. (b) Different V_{ds} at L_{un}=10nm.

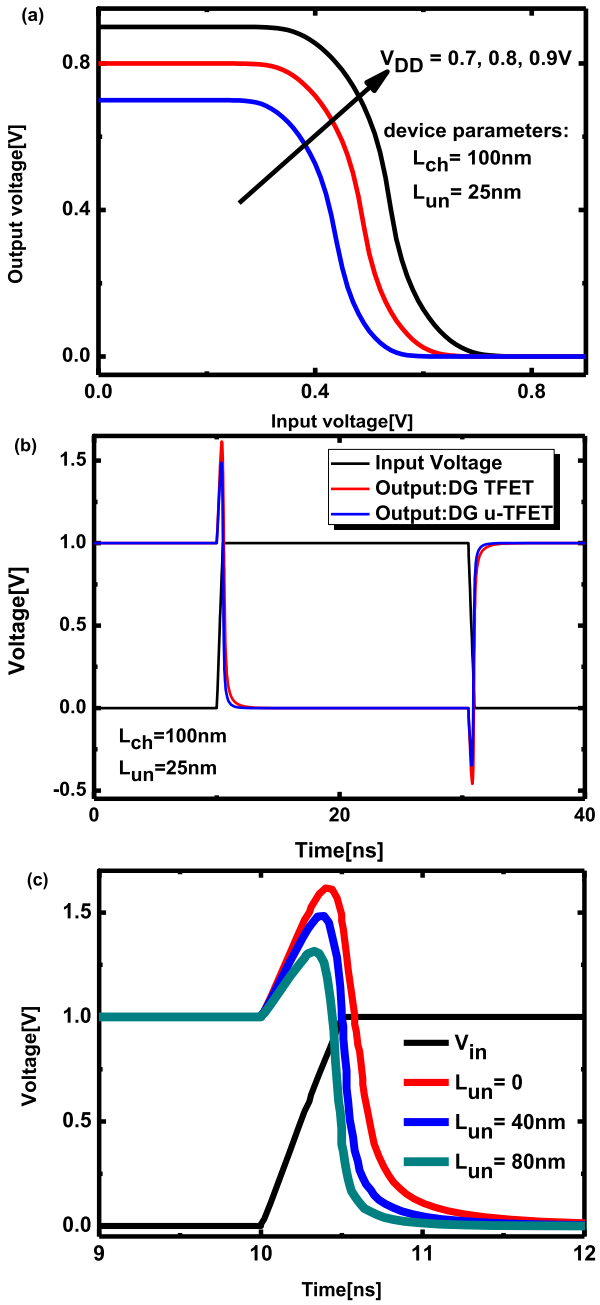

Fig. 8. (a) VTCs of DG u-TFET inverter. (b) Transient response of DG TFET inverter and DG u-TFET inverter. (c) Output voltage overshot (undershot) is alleviated by increasing underlap.

Fig. 4(b) clearly shows the inversion electrons faded by increasing the drain voltage, thus the device works from nonsaturation to saturation region. The model-predicted gate–drain capacitance ($C_{\rm dg}$) is compared with simulation data at different $L_{\rm un}$ in Fig. 5(a). At each underlap distance, the model matches the simulation data very well. The total gate–drain capacitance is decreased with $L_{\rm un}$, and its two components $C_{\rm dg\_inv}$ and $C_{\rm dg\_inf}$ are plotted in Fig. 5(b) and (c). At each operation region, like the channel charge, only one component is dominant. As it can be seen, in saturation region, the inversion layer cannot be generated that $C_{\rm dg\_inv} = 0$. The inner fringe capacitance is also decreased when the device goes into nonsaturation by increasing $V_{\rm gs}$.

The surface potential and ambipolar current are checked for DG u-TFET with $L_{\rm un} = 5$, 10, 20 nm. Also, profiles of DG TFET are also plotted for comparison. As shown in Fig. 6, the model-predicted potential is well matched with the TCAD simulation, proving the correctness of full-depletion assumption in region U. As $L_{\rm un}$ is increased, potential slopes more gently through the underlap region, reducing the inside electric field, thus the carrier tunneling rate is effectively diminished. Since the observed ambipolar current is pretty small and ranges from several orders, the simulation and model-predicted results are extracted from $V_{\rm gs} = -0.5$ V where significant current can be reached. Fig. 7(a) shows that current reduction with more than six orders of magnitude is achieved as the underlap distance is increased from 0 to 20 nm at $V_{\rm gs} = -1.5$ V. With a 20-nm underlap, the ambipolar current is almost negligible under the common operation voltage ($V_{\rm DD} \sim 0.7$ V) as the output voltage undershot is always smaller than $-V_{\rm DD}$. Generally, as shown by the simulation and model results, shorter gate will bring smaller gate–drain capacitance and is more effective for suppressing the ambipolarity, but meanwhile, more drain current degradation. Thus, moderation must be taken, according to the real circuit requirement.

To demonstrate the model flexibility in circuit simulation, it is coded with Verilog-A and implemented into HSPICE. For the sake of simplicity, an inverter is established, and its voltage transfer curves (VTCs) at different supply voltages are shown in Fig. 8(a). Transient response with $V_{\rm DD} = 0.9$ V and a load capacitance $C_{\rm load} = 1$ fF is shown in Fig. 8(b). The output voltage over/undershot is alleviated in DG u-TFET inverter

due to the reduced Miller capacitance [Fig. 8(c)]. There is no convergence problem during the simulation process, demonstrating the model's robustness in the running process.

V. Conclusion

A compact model for DG u-TFET in all operation regions is proposed which reflects the characteristics of the gate–drain underlap on device drain current and Miller capacitance. According to the simulation results of TCAD and HSPICE, the model shows acceptable accuracy and flexibility in circuit simulation. This model provides constructive guidelines to design the gate–drain underlap for TFET and can be further applied to circuit evaluation on the performance boost due to the diminished ambipolar current and Miller capacitance. It is possible that via this model, subsequent works on u-TFET-based circuits will be carried out for future applications.

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